Agilent N4851A/B MIPI D-PHY Acquisition Probes

User's Guide

Agilent Technologies

Notices

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CAUTION

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A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

Contents

1 Introduction

About this Manual

This manual will help you connect an Agilent N4851A/B acquisition probe to your board and set up the logic analysis system to make measurements.

IMPORTANT: Get the Latest Software and Manuals

Agilent Technologies may make further improvements in the software and in this manual.

See "Where to find the software" on page 15 for instructions.

Additional Information Sources

This manual is intended to be used with these other documents:

- See the *Agilent N4851A/B, N4861A/B Probes for MIPI D-PHY Design Guide* for information on how to design the necessary connectors into your board. This document is available by searching for “N4851A” or “N4851B” at www.agilent.com.
- See the *Agilent N4861A/B Stimulus Probes User’s Guide* for information on how to use the N4851A/B acquisition probes and the N4861A/B stimulus probe together.
- See the N4851A/B, N4861A/B product data sheet for a description of the product and its characteristics.
- See the online help in the logic analysis system for more information on using the software tools.

  There is online help for the Image Inserter tool which generates stimulus from an image file and for the Image Extractor tool which converts acquired data into an image file for analysis. Image Inserter and Image Ectractor are parts of the included MIPI Dsi Tools software package.
- Detailed information on Agilent probes (such as the Agilent E5381A differential flying lead probe) is available by searching for the product number at www.agilent.com.
- Additional application notes or white papers may be available from your Agilent representative.

Product Overview

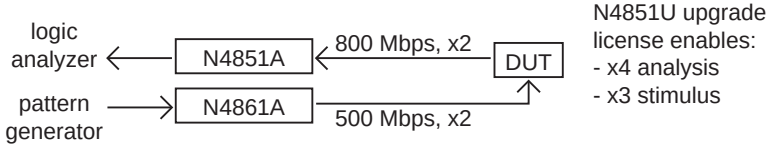
The Agilent N4851A/B acquisition probe connects an Agilent Technologies logic analyzer between the peripheral and baseband components on a device under test (DUT), to allow decoding and display of MIPI D-PHY signals. Software is provided to decode the DSI version 1.01 and CSI-2 protocols.

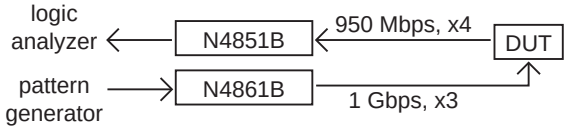
The acquisition probe may be connected to a production board, as long as it incorporates the necessary connectors, or the probe may be connected to a test platform.

The Agilent N4861A/B stimulus probe allows you to generate the digital signals, emulating a master IC. The stimulus probe is usually connected to a test platform which contains only one of the two ICs.

The Agilent N4851U upgrade license lets the N4851A acquisition probe support x4 lanes and the N4861A stimulus probe support x3 lanes. (Supported speeds are the same.)

The "B" models support both faster speeds and a greater number of lanes.





Connection to the device under test

The 90-pin cable on the Agilent N4851A/B acquisition probe is the same as the ones which are used on Agilent 1695x-series logic analyzer cards. This allows you to choose from a variety of probes to make the physical connection. See *Probing Solutions for Logic Analyzers*, available from www.agilent.com/find/logic.

The Agilent N4861A/B stimulus probe is connected to the device under test using four or six SMA cables.

The parts of a measurement system

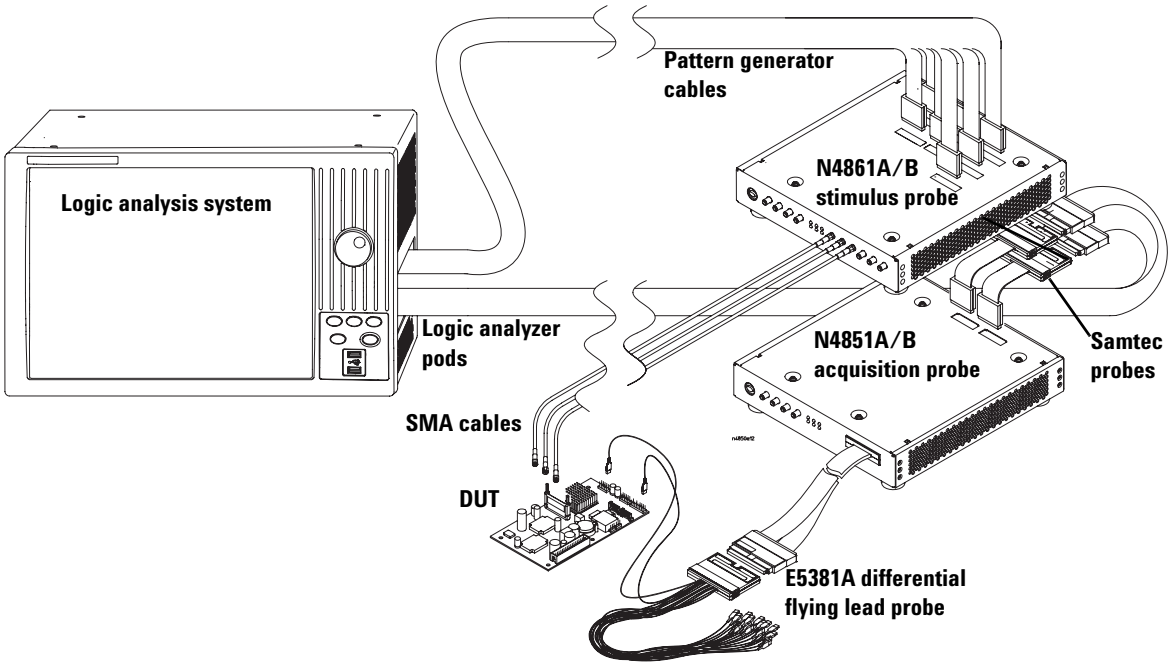


Figure 1 A complete measurement system

The device under test (**DUT**) is your board, which might include an master IC, a slave IC, or both.

The Agilent N4851A/B digital **acquisition probe** captures the digital signal between the sides of a link. A **differential flying lead probe** (or another kind of probe, if needed) connects the DUT to the cable on the acquisition probe.

The Agilent N4861A/B **stimulus probe** can emulate a master IC by supplying the missing digital signals. The stimulus probe connects to the DUT via 50-ohm coaxial cables using SMA connectors.

The acquisition probe and stimulus probe are connected to one another through a short **option cable**.

A **logic analysis system** collects data from the acquisition probe and controls the stimulus probe. The logic analysis system must contain at least one **logic analyzer** card. If you are using the N4861A/B stimulus probe, the logic analysis system must also contain a **pattern generator** card.

Each of the cables coming out of the logic analyzer card is called a **pod**. These pods require adapter cables, called **Samtec probes**, to mate with the connectors on the acquisition probe and stimulus probe.

For some logic analyzers, the logic analyzer card and pattern generator are built in, rather than being separate cards.

Software installed on the logic analysis system decodes the digital data and displays it as decoded packets.

Equipment Supplied

The Agilent N4851A/B includes:

- The Agilent N4851A/B acquisition probe.
- A power supply.
- A power cord appropriate for your country.
- This *User's Guide*.
- Regulatory compliance documents.
- (N4851A only) A software license certificate.

Additional Equipment and Software Required

You *must* have the following additional equipment to use the N4851A/B acquisition probe:

- An Agilent 16800-series or 16900-series logic analysis system.
- An Agilent probe adapter to connect the pods of the logic analyzer to the Samtec connectors on the acquisition probe, such as the Agilent E5385A probe. These are sometimes called “Y adapter cables.”
- An Agilent probe to connect the acquisition probe to the device under test. Probing options are described in the the *Agilent N4851A/B, N4861A/B Probes for MIPI D-PHY Design Guide*.
- The Agilent N4851A/B MIPI D-PHY Digital Acquisition Probe software. See “Installing the Software” on page 15 for information on obtaining and installing the software.

The following equipment and software *may* be required, depending on the kinds of measurements you plan to make:

- An Agilent N4861A/B stimulus probe and associated equipment and software.
- SMA cables, if you will be using the SMA outputs with another instrument.
- A torque wrench for the SMA connectors. The wrench should provide 0.8 to 0.9 N•m (7 to 8 inch-pounds) of torque. An Agilent 3.5mm torque wrench (part number 8710-1765) will provide the appropriate amount of torque.
- The Agilent B4641A protocol development kit for customizing the protocol.

Overview of Installation and Setup

1. Check that you received all of the necessary equipment. See "Equipment Supplied" on page 12 and "Additional Equipment and Software Required" on page 13.
2. Check that the device under test has the necessary connectors. Make sure you know (or can find out) the name and voltage level of the signal at each connector. See the *Agilent N4851A/B, N4861A/B Probes for MIPI D-PHY Design Guide*.
3. Set up the logic analysis system, if necessary.
4. Turn on the logic analysis system.
5. Install the software on the logic analysis system. See "Installing and Configuring the Software" on page 15.
6. Make the physical connections. This includes:
   - Connecting the acquisition probe to the logic analyzer.
   - Connecting the acquisition probe to the device under test.
   - Connecting power to the acquisition probe.
   - Connecting other instruments, such as the N4861A/B stimulus probe or an oscilloscope.
7. Turn on the acquisition probe, then the device under test. See "Connecting the Probe to a Power Source" on page 34.
8. Load a configuration file. See "Loading a Configuration File" on page 18.
9. Set up a logic analyzer trigger. See "Capturing Data" on page 37.
10. Begin making measurements.

2 Installing and Configuring the Software

Installing the Software

Where to find the software

Your Agilent logic analyzer is shipped with the latest application software installed on the instrument, including any licensed optional products you may have purchased.

The latest version of logic analyzer instrument and application software can be downloaded from the web or by ordering a copy of the logic analyzer application CD.

To download the latest logic analyzer application software

The latest logic analyzer product software can be downloaded from the web at:

http://www.agilent.com/find/LA-SW-Download

NOTE While you are visiting the Web site, be sure to download the most recent version of the manuals. You can find the manuals by searching for "N4851A" or "N4851B" at www.agilent.com.

To obtain an application software CD

Logic analyzer product CDs can be ordered from this Web site:

http://software.cos.agilent.com/LogicAnalyzerSW

To sign up for software update notification

To be notified when software upgrades are available for downloading from the web, please sign up for email notification at:

http://www.agilent.com/find/emailupdates

Installing the logic analysis system software

The N4851A acquisition probe requires version 03.70 or higher of the logic analysis system core software.

The N4851B acquisition probe requires version 03.83 or higher.

- If you downloaded the software, double-click **SetupLAxxxxxxxx.exe** then follow the instructions which are displayed.
- If you have a CD, insert the product CD and select **Install Products>Install Agilent Logic Analyzer**, then follow the instructions which are displayed.

Note that newer versions of the Logic Analyzer software will automatically uninstall the previous version as a step in the upgrade. (User files in the "Documents and Settings" folder are not affected.)

To install the logic analyzer software onto your PC for offline processing, insert the product CD into your PC drive, click INSTALL PRODUCTS>Install Logic Analyzer.

Installing the probe software

The packet decoder and packet viewer are included with the N4851A/B acquisition probe. Other software may require a license before it can be used.

- If you downloaded the software, double-click **SetupProbeMIPIxxxxxxxx.exe** then follow the instructions which are displayed.
- If you have a CD, insert the product CD and select **Install Products>Install an Optional Probe>Install Agilent N4851A/B MIPI D-PHY Digital Acquisition Probe MIPI 03.xx.xxxx**, then follow the instructions which are displayed.
- If you will be using any licensed software, follow the instructions on the Entitlement Certificate to install the license. For more information, go to the Index tab in the online help and click “license.”

Installing additional software

If you want to use additional tools then you may need to purchase the proper licenses. For example, if you want to customize the protocol files, you will need the Agilent B4641A protocol development kit, which is licensed.

1. Insert the product CD and select **Install Products**, then install the additional software you need.
2. Follow the instructions on the Entitlement certificate to install the license for the software. For more information, go to the Index tab in the online help and click “license.”

Loading a Configuration File

You configure the logic analyzer by loading a configuration file. The information in the configuration file includes:

- Signal/bus names and channel assignments for the logic analyzer.
- Tool configuration including logic analyzers, probes, filters, and Listing displays.

Several configuration files are provided with the N4851A/B acquisition probe. In most cases, the logic analyzer configuration will be modified to work with your particular DUT, then saved as a custom configuration file.

To choose which provided configuration file to load

Several configuration files are provided. Choose the appropriate configuration for the measurement that you will be making.

Use the configuration files in the Analysis directory if you will be using a N4851A/B acquisition probe without an N4861A/B stimulus probe. Use configuration files in the Stimulus directory if you will be using both probes.

Table 1 Supplied configuration files

Shortcut name	File name	Description
Load CSI2 x1 Analysis Only Default Config	Analysis/CSI2_x1_AnalysisOnly.xml	CSI, 1-Card Analyzer, Data Lane 0 only; for use when N4861A/B is not used
Load CSI2 x2 Analysis Only Default Config	Analysis/CSI2_x2_AnalysisOnly.xml	CSI, 1-Card Analyzer, Data Lanes 0 and 1; for use when N4861A/B is not used
Load CSI2 x1 Stimulus Default Config	Stimulus/CSI2_x1_Stimulus.xml	CSI, 1-Card Analyzer with pattern generator, Data Lane 0 only; used when both analysis and stimulus will be used
Load CSI2 x2 Stimulus Default Config	Stimulus/CSI2_x2_Stimulus.xml	CSI, 1-Card Analyzer with pattern generator, Data Lanes 0 and 1; used when both analysis and stimulus will be used

Table 1 Supplied configuration files (continued)

Shortcut name	File name	Description
Load DSI x1 Analysis Only Default Config	Analysis/DSI_V1_01_x1_AnalysisOnly.xml	DSI 1.01, 1-Card Analyzer, Data Lane 0 only; for use when N4861A/B is not used
Load DSI x2 Analysis Only Default Config	Analysis/DSI_V1_01_x2_AnalysisOnly.xml	DSI 1.01, 1-Card Analyzer, Data Lanes 0 and 1; for use when N4861A/B is not used
Load DSI x1 Stimulus Default Config	Stimulus/DSI_V1_01_x1_Stimulus.xml	DSI 1.01, 1-Card Analyzer with pattern generator, Data Lane 0 only; used when both analysis and stimulus will be used
Load DSI x2 Stimulus Default Config	Stimulus/DSI_V1_01_x2_Stimulus.xml	DSI 1.01, 1-Card Analyzer with pattern generator, Data Lanes 0 and 1; used when both analysis and stimulus will be used

To load a provided configuration file

1. Check that the N4851A/B acquisition probe is connected to the logic analysis system and that it is turned on. See "Connecting to Your Board" on page 27.

   If you load a configuration file with the probe powered off, or not connected or incorrectly connected to the analyzer pods, the communication with the probe will fail and you will see an error message.

2. Close the logic analyzer window, if it is open.

3. Select **Start>All Programs>Agilent Logic Analyzer>Agilent N4851_61A MIPI D-PHY Default Configs** or open the shortcut on the desktop.

4. Click on the configuration you want.

   When you click on a configuration file, the logic analyzer software will start and configure itself.

To load a provided configuration file without restarting the logic analyzer software

1. Check that the N4851A/B acquisition probe is connected to the logic analysis system and that it is turned on. See "Connecting to Your Board" on page 27.

   If you load a configuration file with the probe powered off, or not connected or incorrectly connected to the analyzer pods, the communication with the probe will fail and you will see an error message.

2. Select **File>Open...**.

3. Navigate to the configuration file.

   The default location is:

```
C:\Documents and Settings\All Users\Documents\Agilent
Technologies\Logic Analyzer\Default Configs\Agilent\
N4851_61A\
```

4. Select the file and click Open.

To save a configuration file

The provided configuration files are read-only. If you modify the configuration and want to save your work, select **File>Save As...** and save the configuration as an ALA format file.

ALA format configuration files are more complete and efficient than XML format configuration files. See the logic analyzer online help for more information on these formats.

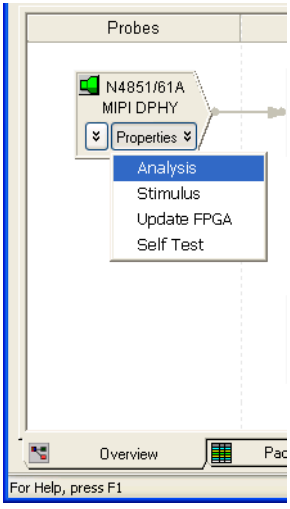
Setting up the Probe for Your Device Under Test

To open the probe setup dialog

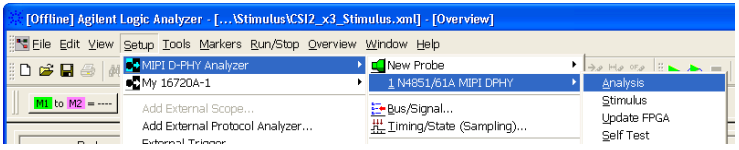
Before you can make any measurements, you need to configure the acquisition probe for the type of link you are probing.

1 Make sure the acquisition probe is connected and turned on. See "Connecting to Your Board" on page 27.

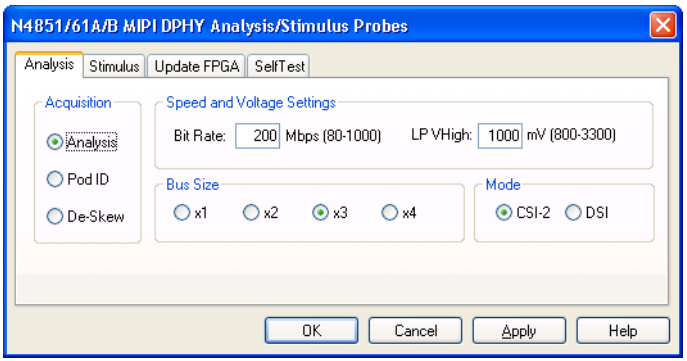
2 Open the Properties dialog:



Or:



3 In the properties dialog's Analysis tab, set the acquisition probe mode. (See "To set the acquisition probe mode" on page 23.)



4 Configure the N4851A/B speed and voltage settings. (See "To configure the clock speed and voltage settings" on page 23.)

5 Configure the N4851A/B bus size. (See "To configure the bus size" on page 25.)

6 Configure the N4851A/B protcol mode. (See "To configure the protocol mode" on page 25.)

7 Configure the N4861A/B stimulus probe settings, as described in the *Agilent N4861A/B Stimulus Probe User's Guide* and in the online help.

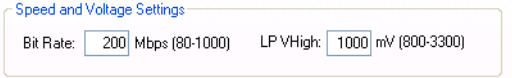
Once you have configured the acquisition probe, remember to select **File>Save As...** and save the logic analyzer configuration.

To set the acquisition probe mode

The probe has these modes of operation:

- **Analysis** — this mode is used to analyze the device under test. Analysis is the "normal" mode for acquiring activity from the link under test. Most of the graphical elements on the Setup tab which control the probe configuration are available only in Analysis mode.
- **Pod ID** — this mode outputs Pod ID values on the analyzer channels and can be used to validate proper connection to the analyzer card. See the online help for instructions on how to do this.
- **De-Skew** — this mode toggles all bits to the analyzer and can be used to validate that the cables are all connected properly and that the proper setup and hold values in the analyzer cards are set. Use the logic analyzer's eye finder with the De-Skew mode to validate that the proper setup and hold values are set. This should not be necessary during normal use. Use De-Skew mode only when instructed to do so by Agilent.

To configure the clock speed and voltage settings



Bit Rate

Set the HS bit rate which is used by your device under test (DUT).

NOTE Make sure you only enter bit rates that your acquisition hardware supports. The N4851A acquisition probe supports bit rates up to 800 Mbps and the N4851B acquisition probe supports bit rates up to 950 Mbps.

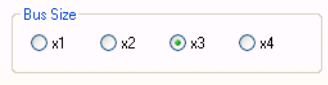
LP VHigh

For LP VHigh, enter the low-power signaling level (the voltage considered to be "high" when the MIPI D-PHY link is operating in LP mode).

The N4851A/B acquisition probe uses the threshold (LP VHigh / 2) to detect LP mode.

NOTE **Do not change the voltage thresholds in the logic analysis system's Bus/Signal Setup dialog.** The voltage levels of the signals from the N4851A/B acquisition probe to the logic analyzer are always the same and never need to be adjusted. To adjust for the voltage levels on your DUT, use the probe setup dialog.

To configure the bus size

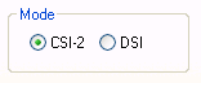


Select the bus size:

- x1 – acquires data from one lane (Data Lane 0).
- x2 – acquires data from two lanes (Data Lane 0, 1).
- x3 – acquires data from three lanes (Data Lane 0, 1, 2).
- x4 – acquires data from four lanes (Data Lane 0, 1, 2, 3).

The x3 and x4 options are available with the N4851B acquisition probe or when the N4851U upgrade license has been installed with the N4851A acquisition probe.

To configure the protocol mode



Select CSI-2 or DSI.

3 Connecting to Your Board

To connect the N4851A/B acquisition probe to the device under test (DUT), follow these steps:

1. Check that the device under test has the necessary connectors, as specified in the *Agilent N4851A/B, N4861A/B Probes for MIPI D-PHY Design Guide*.
2. Make sure you know the name and voltage level of the signal at each connector.
3. Check the signal quality at each connector with an oscilloscope. See "Checking signal integrity" on page 28.
4. Position the N4851A/B acquisition probe for easy access and good ventilation. See "Positioning the Probe" on page 28.
5. Connect the logic analyzer cables to the N4851A/B acquisition probe. See "Connecting to the Logic Analysis System" on page 29.
6. Connect the acquisition probe to each of the required signals, listed in Table 2 on page 32.
7. Turn on the logic analysis system, then the N4851A/B acquisition probe, then the DUT. See "Connecting the Probe to a Power Source" on page 34.

8 Perform initial checks to confirm that the acquisition probe is ready to capture valid data:

a Check the LEDs on the front of the acquisition probe. See "Understanding the LEDs" on page 62.

Checking signal integrity

The N4851A/B acquisition probe is designed to be used with signals that meet the MIPI D-PHY electrical requirements. Before you connect the N4851A/B acquisition probe to your signals, use an oscilloscope to check the signals.

Positioning the Probe

Take care to allow space for the probe be placed near the device under test and the logic analysis system. You will also need plenty of space near the probe for the logic analysis system.

See "Mechanical Characteristics" on page 67 for probe dimensions.

Position the probe and power supply so that it is not difficult to unplug the power cord.

Allow at sufficient clearance above the probe for the logic analyzer cables. You may stack the N4861A/B stimulus probe on top of the N4851A/B acquisition probe.

Allow at least 5 cm (2 in) clearance on both sides of the probe for proper cooling.

CAUTION Do not block the airflow holes on the sides of the probe box. Blocked airflow may cause overheating and equipment damage

Connecting to the Logic Analysis System

The N4851A/B acquisition probe has two slots along the top edge labeled "Pod 1/Pod 2" and "Pod 3/ Pod 4". These slots are where the analyzer pods connect to the probe. Use the appropriate Samtec probe adapter to connect the probes to your logic analyzer card.

Logic analyzers with 90-pin connectors

Many logic analyzer cards, such as those in the 1695x family, have 90-pin connectors at the end of the pod cables. Use two E5378A 90-pin to Samtec probe adapters to connect the logic analyzer card to the probe.

- Connect Pod 1 to the Odd side of Pod 1 / Pod2.
- Connect Pod 2 to the Even side of Pod 1 / Pod 2.
- Connect Pod 3 to the Odd side of Pod 3 / Pod 4.
- Connect Pod 4 to the Even side of Pod 3 / Pod 4.

Logic analyzers with 40-pin connectors

If you are using a 40-pin connector based logic analyzer card then you will need to use two E5385A 40-pin to Samtec probe adapters. Connect them as listed above.

To verify the logic analyzer connections

If you are unsure whether you have connected the logic analyzer pods to the correct connectors on the N4851A/B acquisition probe, use the probe's Pod ID mode.

1. Turn on the logic analysis system and the N4851A/B acquisition probe.
2. Display the N4851/61A MIPI DPHY probe tool.
3. In the Setup tab, select Pod ID mode.
4. Open the logic analyzer's Bus/Signal Setup window.
5. Find the signal activity indicators next to the bus/signal names.
6. Examine the activity indicators to determine if the pod is connected to the right place on the acquisition probe. At each connector on the acquisition probe, the "activity" pattern of bits will be a binary value that corresponds to the pod number.

Pod ID mode requires that at least one of the pods has been connected correctly.

Connecting to the Device Under Test

The probe uses the same 90-pin probe cable as the Agilent 1695x-series logic analyzer. That allows you to choose from a variety of probes to make the physical connection.

CAUTION

Caution: input connector

Connect the probe cable only to an Agilent Technologies probe, following the design recommendations in the *Agilent N4851A/B, N4861A/B Probes for MIPI D-PHY Design Guide*.

Do not connect the signals or grounds to high voltages. Use ESD precautions to avoid static discharge. The grounds are not isolated from earth ground. Applying voltages which are above 5 V could damage the N4851A/B acquisition probe.

The exact details of the physical connection depend on which probe you use. See the *Agilent N4851A/B, N4861A/B Probes for MIPI D-PHY Design Guide* and the manual for the probe you are using.

Signal-to-channel mapping

The following table shows the default mapping of signal names to logic analyzer channel numbers. This mapping works well if you are using Agilent E5381A flying leads.

Table 2 Connections for E5381A flying leads

Signal	Logic analyzer lead to connect	Comments
Clkp	Ch 15, positive	Ground N side of differential probe.
Clkn	CLOCK, positive	Ground N side of differential probe.
VSense	Ch 6, positive	Required if using the N4861A/B stimulus probe. Optional if using the N4851A/B acquisition probe alone. Ground N side of differential probe.
Data Lane 0p	Ch 8, positive	Ground N side of differential probe.
Data Lane 0n	Ch 9, positive	Ground N side of differential probe.
Data Lane 1	Ch 10	Probe differentially
Data Lane 2	Ch 11	Supported by N4851B. Supported by N4851A with N4851U upgrade license. Probe differentially
Data Lane 3	Ch 12	Supported by N4851B. Supported by N4851A with N4851U upgrade license. Probe differentially

The Data Lane 0p, Data Lane 0n, Clkp, and Clkn lines are probed both as single ended and differential, even though the your physical connection is only single ended. This is done to allow the logic analyzer to detect LP and HS modes. The negative sides of all of these connections *must* be connected to ground.

Lanes 1, 2, and 3 are probed by a single differential channel.

Connecting the SMA cables (optional)

Threaded SMA connectors are provided in case you want to view the signals with another instrument, such as an oscilloscope.

S3 S3 is high (3.3V) when Data Lane 0 is in High Speed mode.

S2 S2 is high (3.3V) when Clk is in High Speed mode.

CAUTION

Caution: SMA connectors

The SMA outputs are 3.3V only. Do not connect short these connectors to ground or to other low-impedance sources.

Do not connect the grounds to a high voltage—the grounds are not isolated from earth ground. When working near the SMA connectors, use ESD precautions to avoid static discharge.

Failure to follow these precautions could damage the N4851A/B acquisition probe.

Use a torque wrench to tighten the SMA connector.

Apply 0.8 to 0.9 N•m (7 to 8 inch-pounds) of torque. An Agilent 3.5 mm torque wrench (part number 8710-1765) will provide the appropriate amount of torque.

Some torque wrenches, such as the Agilent SMA torque wrench (part number 8710-1582) provide only 5 in-lbs of torque. If you apply too little torque, the electrical connection may not be reliable.

CAUTION

Apply no more than 0.9 N•m (8 inch-pounds) of torque. If you apply too much torque, the N4851A/B acquisition probe may be damaged.

Connecting the Probe to a Power Source

The probe is shipped from the factory with a power supply and cord appropriate for your country. If the cord you received is not appropriate for your electrical power outlet type, contact your Agilent Technologies sales and service office.

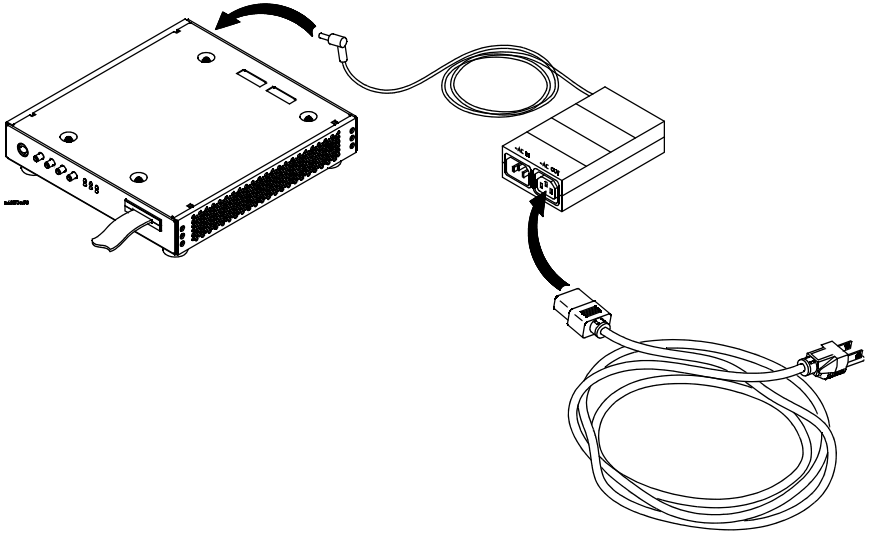
Position the probe and power supply so that it is not difficult to unplug the power cord.

WARNING **Maintain ground to avoid electrical shock.** Use only the power supply and power cord supplied with the probe. Connect the power cord only to a properly grounded electrical power outlet.

1 Connect the power cord to the power supply and to a socket outlet.

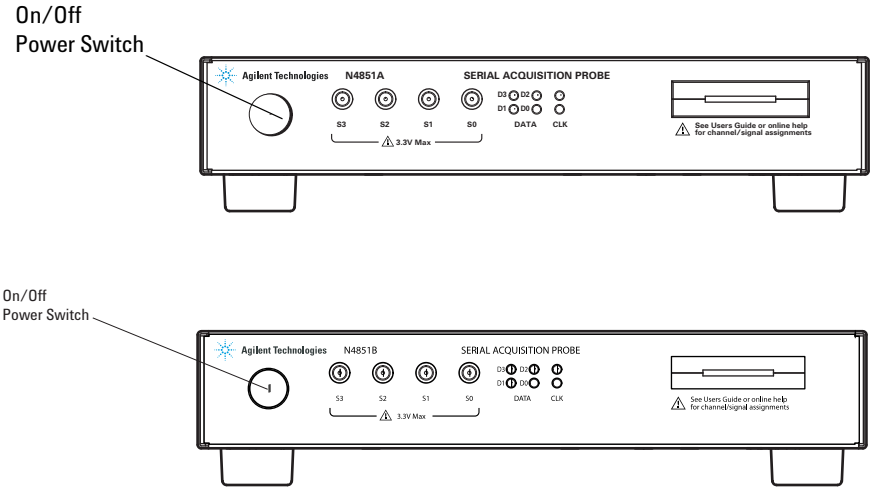
2 Connect the 12V power cord to the back of the probe.

Ensure the power supply plug is completely seated in the power input receptacle.



To turn power ON

- Press the power button on the front of the probe.



The power button is lighted when the switch is ON.

It is best to power on the probe *before* loading a configuration file into the logic analysis system.

You may turn the probe on before or after the logic analysis system is turned on. You may connect and disconnect the cables and the logic analyzer pods while the probe and logic analyzer are powered on.

When you turn on the probe, self-test and loading of calibration factors can take up to 45 seconds.

To turn power OFF

- Press the power button on the front of the probe.

4 Capturing Data

This chapter shows you how to set up logic analyzer triggers to capture just the data you want.

The normal steps in using the logic analyzer are:

1 Configure the logic analyzer.

2 Configure the probe for the measurement.

3 Set up the trigger, and run the measurement.

4 Display the captured data.

The logic analyzer is configured, and buses (sometimes known as "labels") are created for the logic analysis signals when configuration files are loaded (see "Loading a Configuration File" on page 18).

Is the data captured in real time?

The logic analyzer captures data in real time as it is running. The trigger stops the measurement, after which you can use various tools to view the data which has been stored in the logic analyzer's memory.

This chapter describes setting up logic analyzer triggers. See "Viewing the Captured Data" on page 47 for information on displaying the captured data.

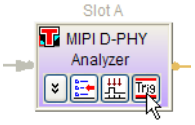
Triggering on a High-Speed Packet

You can set up the logic analyzer to trigger when a certain event happens. For example, you can set the logic analyzer to trigger:

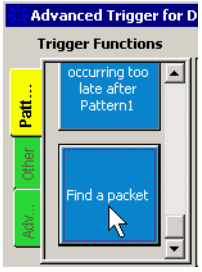
- When a certain kind of packet is detected.
- When a field in the header of a packet has a particular value.
- When the first few bytes of the payload has a particular value.
- When an error condition is detected.

To trigger on a high-speed packet:

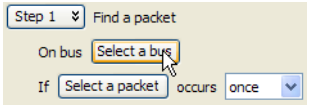
1 Open the Advanced Trigger dialog for the appropriate analyzer.

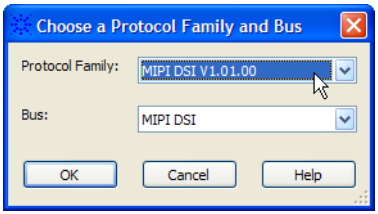


2 In the Advanced Trigger dialog, scroll down the list of trigger functions and drag **Find a packet** into the trigger sequence.

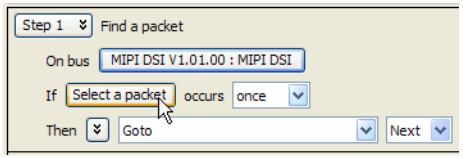


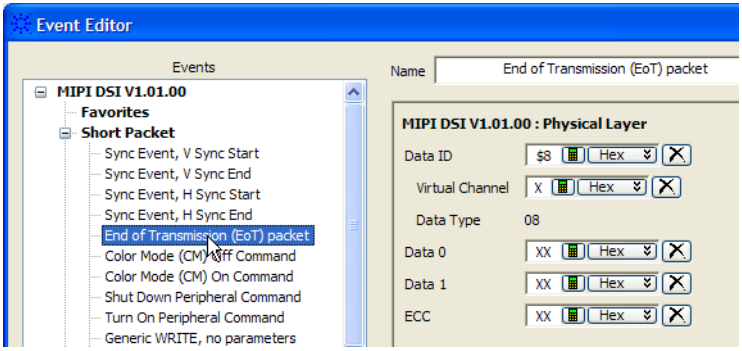
3 Select the bus.





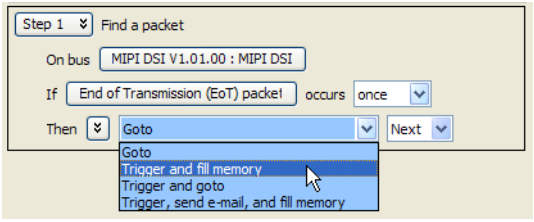
4 Select the packet which the logic analyzer should watch for.





5 If you want the logic analyzer to trigger only when the value of a field in the packet header has a certain value, or when the packet payload begins with a certain value, enter the value. Leave the value as “X” to trigger on any value.

6 Select what the logic analyzer should do when it encounters the packet. Usually you will want to "Trigger and fill memory."



7 If you want to capture activity which happened before the trigger, or if you want to reduce the amount of information which is captured, see "To adjust sample position and memory depth" on page 43.

8 Click **OK**.

9 Run the logic analyzer.

To add new events

You cannot *modify* the events and packet types which are supplied in the configuration files, but you can *add* events using the Event Editor.

Triggering On Specific Events

To trigger on a standard D-PHY sequence error

The only standard D-PHY sequence error which is directly detected by the logic analysis system is SoT Sync Error. To trigger on this error:

1. In the Advanced Trigger dialog, select the LaneErr Bus/Signal for the lane of interest.
2. Select “All bits” and “=”.
3. Change the base to Symbols.
4. Select the SoT Sync Error symbol.

Figure 2 Standard DPHY Sequence Errors

Error	Description	Logic analyzer support
SoT Error	The Leader sequence for Start of High-Speed Transmission is fault tolerant for any single-bit error and some multi-bit errors. Therefore, the synchronization may be usable, but confidence in the payload data is lower. If this situation occurs an SoT Error is indicated.	Not Implemented
SoT Sync Error	If the SoT Leader sequence is corrupted in a way that proper synchronization cannot be expected a SoT Sync Error is indicated.	LaneErr:110

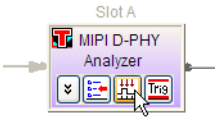
Figure 2 Standard DPHY Sequence Errors (continued)

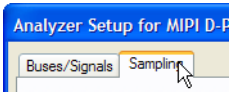
Error	Description	Logic analyzer support
EoT Sync Error	The EoT Sync Error is indicated when the last bit of a transmission does not match a byte boundary. This error can only be indicated in case of EoT processing on Detection of LP-11.	Not Implemented
Escape Mode Entry Command Error	If the receiving Lane Module does not recognize the received Entry Command for Escape an Escape mode Entry Command Error is indicated.	Not Implemented
LP Transmission Sync Error	At the end of a Low-Power Data Transmission procedure, if data is not synchronized to a Byte boundary an Escape Sync Error signal is indicated.	Not Implemented
False Control Error	If a LP-Rqst (LP-10) is not followed by the remainder of a valid Escape or Turnaround sequence, a False Control Error is indicated. This error is also indicated if a HS-Rqst (LP-01) is not correctly followed by a Bridge (LP-00).	Not Implemented

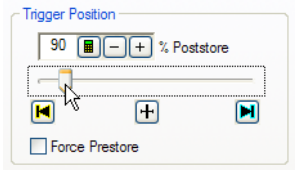
Customizing a Trigger

To adjust sample position and memory depth

If you want to capture activity which happened before the trigger, or if you want to reduce the amount of information which is captured, use the logic analyzer's Sampling tab.







If you move the trigger position, make sure that Force Prestore is not enabled.

To choose which data to store

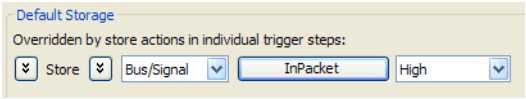
You can control how much data is captured by the analyzer by using storage qualification to store only selected kinds of states.

Storage qualification acts as a real-time filter which allow you to selectively remove states from the captured data.

Example: To discard “status only” data

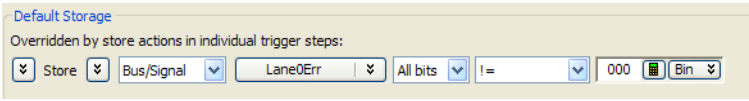
The N4851A/B acquisition probe issues logic analyzer states not only for packet data, but also for codes which indicate changes in status and error bits. These “status only” states indicate the current status of the physical layer bus.

If you do not need this status information, you can choose to store only the HS and LP data. This will allow you to capture significantly more data. To do this, use storage qualification and the InPacket signal.



Example: To store only data lane 0 error states

Use storage qualification and the Lane0Err bus to set up the logic analyzer to store only those states in which the N4851A/B acquisition probe detected an error (such as a time violation or a bus turnaround which was requested but not acknowledged) on data lane 0.



When to Use the Sampling Tab

You may safely use the logic analyzer's Analyzer Setup window to change:

- Trigger position (start/center/end)
- Sampling positions (after running eye finder, to "fine-tune" the results if necessary)
- Acquisition depth

Many of the settings are set by the configuration files and should not be modified. *Do not* use the Analyzer Setup window to change:

- Analyzer mode (state/timing/eye scan)
- Clock setup
- Acquisition speed

5 Viewing the Captured Data

Understanding the Displays in the Logic Analysis System

To display an overview of tools in the logic analysis system

1 At the bottom of the logic analyzer window, click the **Overview** tab.

The Overview window lets you view how the data is sent from the logic analyzer data acquisition module to post-processing tools and display windows. Each icon represents a hardware or software tool you can use. The arrows represent the flow of data between tools.

The **Probes** column shows the probes which physically acquire the data.

The **Modules** column shows the logic analyzer cards which capture the data.

The **Tools** column shows post- processing tools which manipulate the captured data before it is displayed.

The **Windows** column shows the different display windows which you can use to display the captured data.

Tools may be accessed by clicking on their icon, by clicking on the tab at the bottom of the screen, or through the menus at the top of the screen.

See the online help in the logic analysis system for more information on how to add more tools and display windows. The online help also explains how to control the data flow between tools and windows, and how to control the appearance of the data within each window.

Overview window example

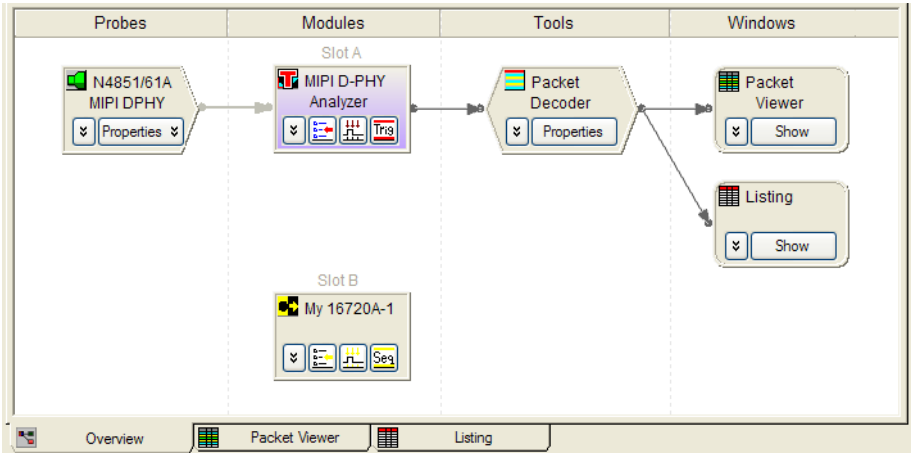


Figure 3 Overview display

Figure 3 on page 48 shows a basic setup for the N4851A/B acquisition probe. The N4851A/B acquisition probe sends data to one logic analyzer (which is probably one-half of a logic analyzer card, set up as a “module”). The data is decoded by the MIPI D-PHY decoder tool.

The decoded data is then displayed as a series of logic analyzer states in the Listing window. The data is also displayed in packet form in the Packet Viewer window.

Using the Listing Display

Predefined buses and signals

The configuration files define the following buses and signals. Each bus or signal corresponds to a column in the Listing display.

Table 3 Buses and signals

Signal/bus name	Size in bits	Description
Byte 0(/1/2/3)	8	
SoP	1	
InPacket	1	
LnDir	1	
EoP	4	
ClkErr	2	
LP	2	
LnMode	2	
Lane0(/1/2/3)Err	3	
MIPI CSI-2 CRC Check Lane Data	216	CSI-2 Only

Predefined symbols

Table 4 ClkErr Symbols

Symbol	Value	Description
OK	00	No errors detected
Clk Startup Error	01	LPX min. time violation or CLK-PREPARE + CLK-ZERO min. time violation
T-EOT Error	10	EOT max time violation
Clk to Data Error	11	CLK-POST + EOT min. time violation or CLK-PREPARE min. time violation

Table 5 LaneErr Symbols

Symbol	Value	Description
OK	0	No errors detected
Lane Startup Error	001	LPX min. time violation or HS-PREPARE + HS-ZERO min. time violation
HS-TRAIL Error	010	EOT max time violation
LP Seq. Error	011	LPX min. time violation in low power state
	100	not used
101	101	Bus turnaround error. Bus turnaround was requested, but not acknowledged.
SoT Sync Error	110	HS mode was entered then exited, but no HS sync was detected.

Table 6 LnMode Symbols

Symbol	Value	Description
ULPM	00	In ultra low power state
HSDT	01	High speed data transmission
LPDT	10	Low power data transmission
Stop	11	In stop state

Table 7 LP Symbols

Symbol	Value	Description
Bridge	00	In low power bridge state
HS-Rqst	01	In high speed request state
LP-Rqst	10	In low power request state
Stop	11	In stop state

Selecting a Protocol

You must configure the packet decoder for the protocol being used by the DUT. You can use the Packet Decode Properties dialog to configure:

- Protocol family (CSI-2 or DSI).
- CRC Error Checking (via the Protocol Family selection).
- Number of lanes (via the Decode Bus selection).

The protocol and number of lanes is automatically configured if you load one of the provided configuration files. CRC error checking is enabled by default.

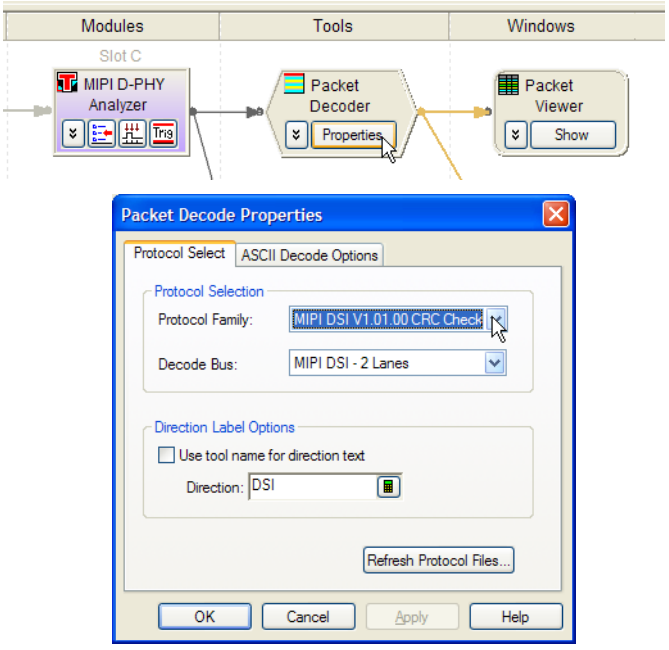


Figure 4 Packet Decoder Properties dialog

To disable ECC/CRC error checking

The CSI-2 and DSI protocols provide for ECC and CRC codes.

If you see numerous errors in the Packet Viewer display, you can turn off error checking by changing a Protocol Family without CRC Checking.

Using the Packet Viewer Display

The Packet Viewer display provides numerous ways to view packet data.

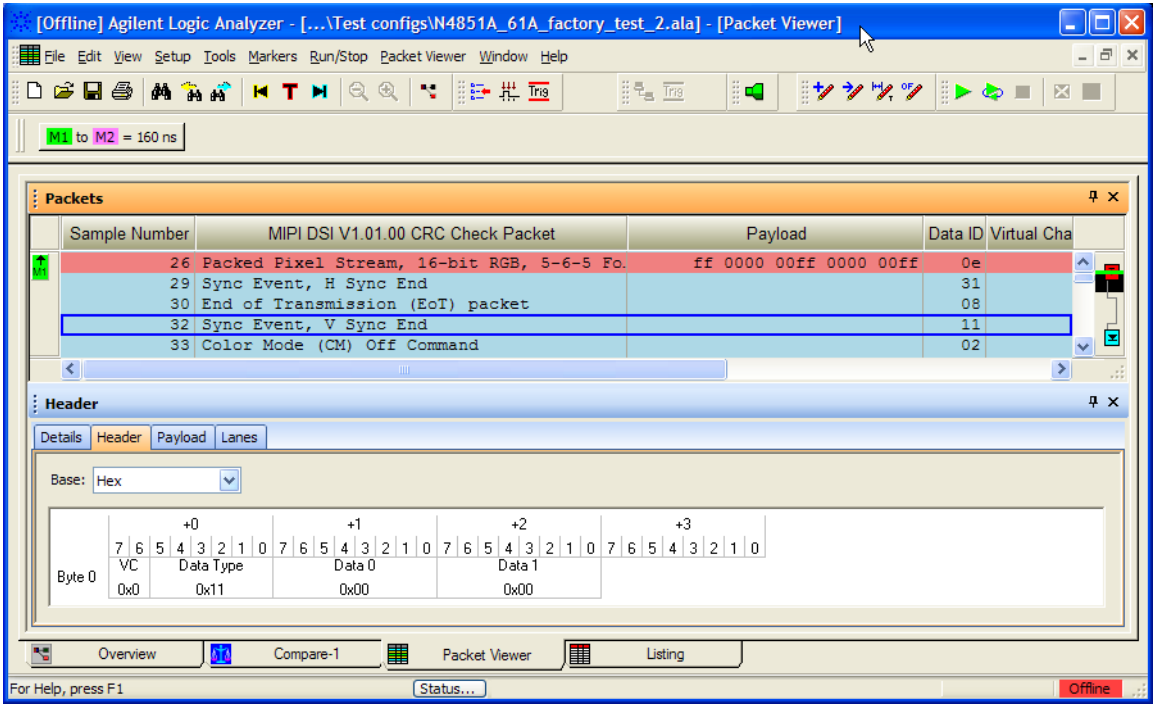


Figure 5 Packet Viewer display

See the online help for information on how to use the Packet Viewer.

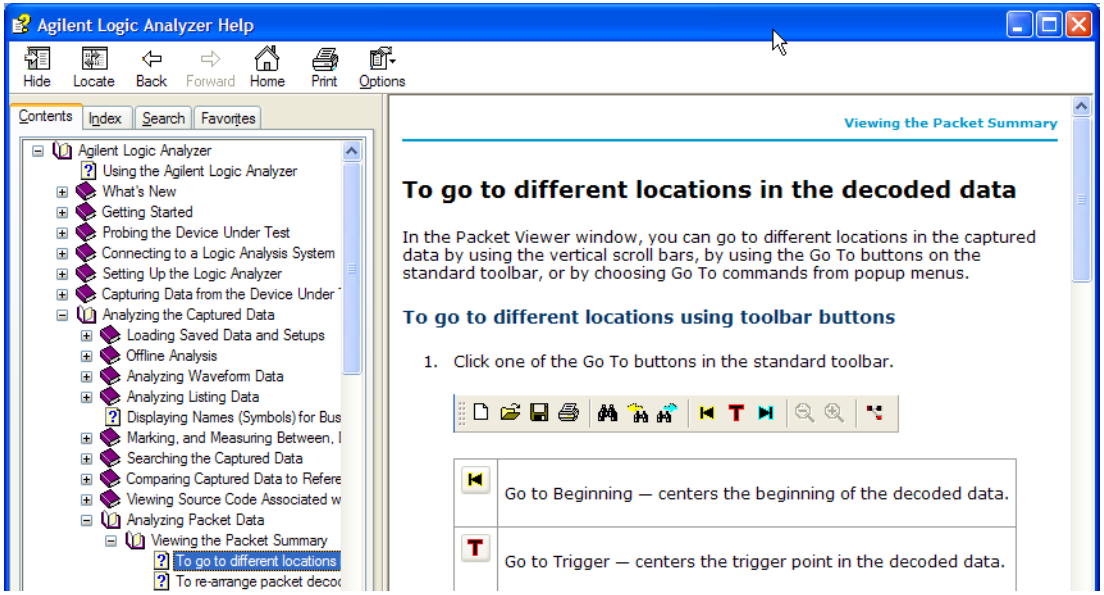


Figure 6 Help for the Packet Viewer

Viewing LP Data

Normally, you would view LP data using the Listing display.

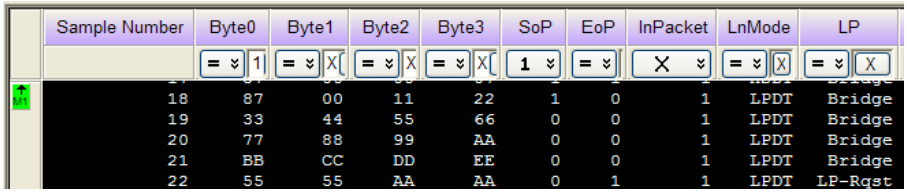


Figure 7 LP data in the Listing display

You may also view LP data with the Packet Viewer. Note that in x2 mode, the data will appear to have been transmitted in packets on both lanes, when in fact it is always transmitted on Data Lane 0.

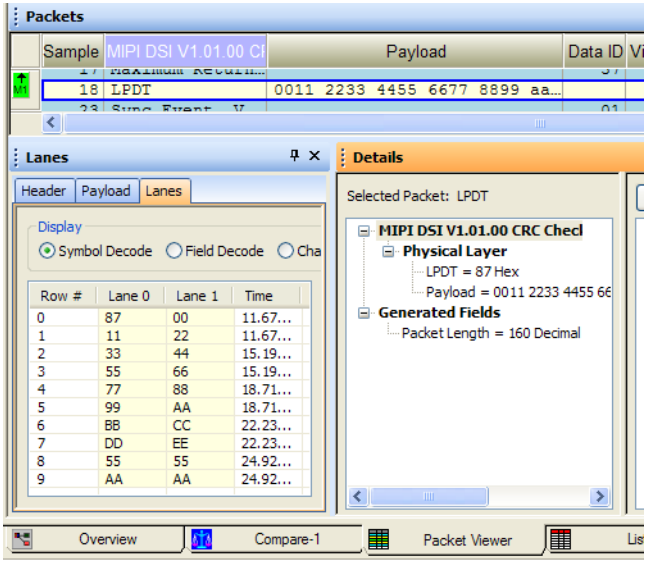


Figure 8 LP data in the Packet Viewer display

6 Customizing the Protocol

Customizing frame structure and command encoding

It is possible to customize the protocol used by the Packet Decoder tool. For example, if your DUT defines additional interface control commands, you could customize the protocol so that those commands will be properly displayed in the Packet Viewer.

Tools required

To customize the protocol, you must have licenses for both the protocol (supplied with the N4851A/B acquisition probe) and the Agilent B4641A protocol development kit (purchased separately).

Protocol description files

The protocol is defined in a set of protocol description files.

Protocol description files are loaded when the Agilent Logic Analyzer application starts or when "refreshed" in the Packet Decoder tool.

Protocol description files have the .aex (Agilent Encrypted XML) file extension.

The Agilent B4641A protocol development kit (PDK) allows you to edit these files. The PDK editor provides standard text editing and XML syntax highlighting features.

See the logic analysis system's online help for step-by-step information on how to edit protocol descriptions.

7 Troubleshooting

Common Problems and Solutions

If you see an error message while loading a configuration file

If you load a configuration file with the probe powered off, or not connected or incorrectly connected to the analyzer pods, the communication with the probe will fail and you will see an error message.

- ✔ Check that the probe is powered on.
- ✔ Check that the probe is connected to the logic analysis system.

If the last packet in the Packet Viewer has an error

The logic analyzer stops storing information when its memory is filled or when the analyzer halts. This will often result in the last packet being cut off before it has been

completely captured. This in turn causes the Packet Viewer to display the message, “Unexpected End Of Packet” at the end of the trace.

If triggers are sometimes missed

If you are sure that the condition you want to trigger on is occuring, but the logic analyzer fails to trigger:

- ✔ Check that the trigger has been set up correctly.
- ✔ If the sample position is not “100% prestore”, check that Force Prestore is not enabled.

To run the built-in self test

1. In the logic analysis system, open the N4851A/B acquisition probe’s Self Test dialog.
2. Select the appropriate test.
3. Follow the directions listed for the test.
4. Click Run Self Test. The results of the test will be displayed.

If an error occurs during Self Test, select "Enable Log to File" and choose a file name, then run the test again.

If the clock is not being acquired correctly

If the clock is AC coupled at the source, you must also place a DC blocking capacitor after the point where the acquisition probe is connecting to the signal. See the *Agilent N4851A/B, N4861A/B Probes for MIPI D-PHY Design Guide* for more information.

If no data is being acquired by the logic analyzer

- ✔ Check that the probe is connected to the correct signals.
- ✔ Check that the logic analyzer is set to trigger on something which you are certain will occur.
- ✔ Use an oscilloscope to check all of the signals while the probe is connected. Check the signal quality. Also check that the probe is not pulling up the center voltage for the differential signals.

If no packets are shown in the Packet Viewer

If the DUT has link or signalling problems, no packets will be displayed. Instead, the Packet Viewer will continue searching the captured data for a packet to display.

Use the Listing display to confirm that this is the case. In the Listing display:

- ✔ Is any data being captured? If not, see "If no data is being acquired by the logic analyzer" on page 61.
- ✔ Do you see any packet headers? Remember, the Sync fields are not captured by the logic analyzer.

If you see packets in the Listing display but not in the Packet Viewer display:

- ✔ If the packets are different in any way from standard MIPI D-PHY packets, you may need to customize the protocol definition file which is used by the Packet Viewer. See "Customizing the Protocol" on page 57.
- ✔ In the Overview display, check that the Packet Viewer is connected to the correct logic analyzer.

Understanding the LEDs

Each of the six LEDs on the front of the N4851A/B acquisition probe can be green, amber, or red.

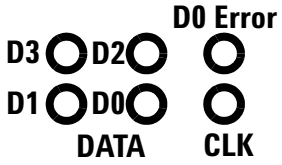


Figure 9 Names of the status LEDs

Table 8 What the colors of the LEDs mean

	D0/D1/D2/D3	CLK	D0 Error
Green	Data lane is in High Speed mode	Clock is in High Speed mode	
Flashing green	Data lane is in Low Power mode		
Amber	Data lane is in Ultra-Low Power state	Clock is in Ultra-Low Power state	
Flashing amber	Data lane is in Stop state		
Red			Error detected on Data Lane 0
Flashing red			
Off	Data idle, no activity	No Clock	

If all LEDs are amber, the probe is in a reset state.

What to look for

When you connect the acquisition probe to the DUT, check the following things:

- ✔ Check CLK first. The CLK LEDs should be steady green.
- ✔ Check the data LEDs. The LED for each lane should be steady green, flashing green, or off.
- ✔ Look for red or “hints of red.”

  Red is always “bad.”

  Amber is combination of red and green. It can be difficult to see a difference difference between amber and intermittent red. But if everything is connected properly, you should not see amber for the data LEDs.

Updating the Firmware

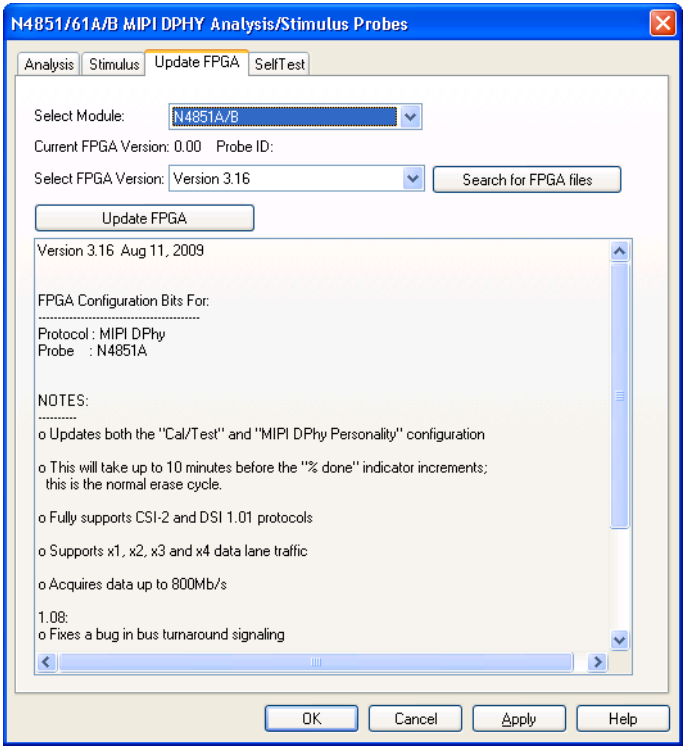
You can update the FPGAs in the probe by sending new configurations over the analyzer cables. It takes up to 60 minutes (the FLASH memory erase time is variable) to update the FPGAs. This should only be done when requested by Agilent.

1. Copy the new firmware to the logic analysis system. Save the files in the following directory:

```
C:\Program Files\Agilent Technologies\Logic Analyzer\AddIns\
   Agilent\N4851A\FPGA
```

2. Check that the N4851A/B acquisition probe is turned on and connected to the logic analysis system.

3 Open the N4851/61A/B MIPI DPHY probe Properties dialog.



4 Select the **Update FPGA** tab.

5 Select the module you wish to update and then which FPGA version you want to use.

6 Click **Update FPGA**.

8 Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics.

These characteristics are subject to change. Information in the product data sheet takes precedence over any information listed here.

Table 1 Protocols supported

Protocol	Version supported
MIPI D-PHY	version 0.9
CSI-2	version 1.00
DSI	version 1.01 (version 1.00 is not supported)

Table 2 N4851A/B Connectors

Connector	Characteristics
Input	Connectors for use only with an Agilent probe. High Speed Mode: Maximum bit rate, N4851B: TBD (see product data sheet on Agilent web site for latest characteristics) Maximum bit rate, N4851A: 750 Mbps Minimum bit rate: 80 Mbps VHigh: 150 mV to +450 mV VLow: –17 mV to +217 mV, (changes with LPVlow or HSVhigh) Low Power Mode: Maximum bit rate: 10 Mbps Minimum bit rate: 800 Kbps VHigh: 0.8 V, to 3.3 V, Max current 24 mA VLow: –100 mV to +100 mV Minimum voltage swing: Complies with MIPI D-PHY requirements Installation category: CAT I (Mains isolated)
SMA S0, S1, S2, S3	SMA S2, S3: output connector for oscilloscope or other instruments SMA S0, S1: connector reserved for future use. (Input/output function configured in firmware). Min: 0.8 V, Max: 3.3 V, Max current 24 mA DC-50 MHz. CAT I (Mains isolated)
Option Connector	Reserved for use with the Agilent N4861A/B stimulus probe.
Logic Analyzer Pod Outputs	Two 38-pin Samtec connectors

Table 3 Electrical Characteristics

Electrical Characteristics	
Power Requirements (Power Supply)	Input: 100-240 V, 1.5 A, 50/60 Hz, IEC 320 connector Output: 12 V, 5 A
Power Requirements (N4851A Probe)	Input: 12 V DC, 5 A. Use only with the provided power supply.
Load Model	See the documentation for the probe you are using.

Table 4 Mechanical Characteristics

Mechanical Characteristics	
Weight	Probe: 2.0 kg (4.4 lb), not including power supply
Analysis Probe Dimensions	See "Positioning the Probe" on page 28 for ventilation requirements.

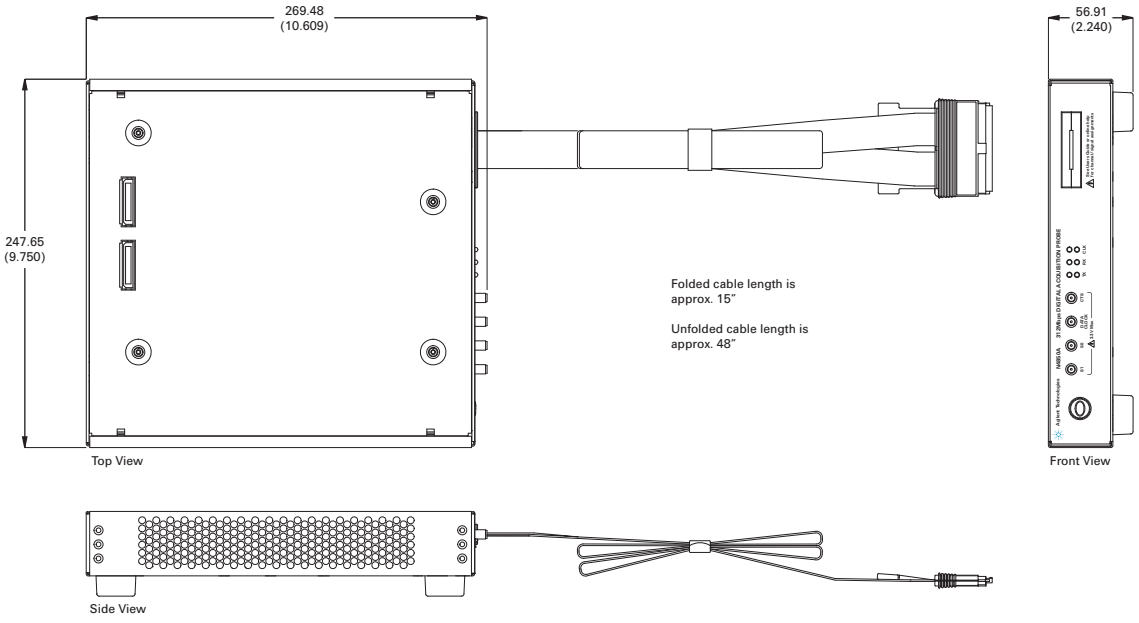


Table 5 Environmental Characteristics (Operating)

Environmental Characteristics (Operating)	
Temperature	Operating/non-operating: +0° to +55° C (+32° to +131° F)
Altitude	Operating/nonoperating 3000 m (10,000 ft)
Humidity	8 to 80% relative humidity at 40° C (104° F). Avoid sudden, extreme temperature changes which could cause condensation on the circuit board. For indoor use only. Pollution degree 2: Normally only dry non-conductive pollution occurs. Occasionally a temporary conductivity caused by pollution may occur.

9 Safety Notices

This apparatus has been designed and tested in accordance with IEC Publication 61010-1, Safety Requirements for Measuring Apparatus, and has been supplied in a safe condition. This is a Safety Class I instrument (provided with terminal for protective earthing). Before applying power, verify that the correct safety precautions are taken (see the following warnings). In addition, note the external markings on the instrument that are described under "Safety Symbols."

Warnings

- Before turning on the instrument, you must connect the protective earth terminal of the instrument to the protective conductor of the (mains) power cord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. You must not negate the protective action by using an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.
- Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short-circuited fuseholders. To do so could cause a shock or fire hazard.
- If you energize this instrument by an auto transformer (for voltage reduction or mains isolation), the common terminal must be connected to the earth terminal of the power source.

- Whenever it is likely that the ground protection is impaired, you must make the instrument inoperative and secure it against any unintended operation.
- Service instructions are for trained service personnel. To avoid dangerous electric shock, do not perform any service unless qualified to do so. Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.
- Do not install substitute parts or perform any unauthorized modification to the instrument.
- Capacitors inside the instrument may retain a charge even if the instrument is disconnected from its source of supply.
- Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.
- Do not use the instrument in a manner not specified by the manufacturer.

To clean the instrument

If the analysis probe requires cleaning: (1) Remove power from the instrument. (2) Clean the external surfaces of the instrument with a soft cloth dampened with a mixture of mild detergent and water. (3) Make sure that the instrument is completely dry before reconnecting it to a power source.

Do not clean the cables.

Safety symbols

"Caution" or "Warning" risk of danger marked on product. See "Safety Notices" on page 2 and refer to this manual for a description of the specific danger.

Hazardous voltage symbol.

Earth terminal symbol: Used to indicate a circuit common connected to grounded chassis.

9 Safety Notices

10 Glossary

For more terms, see the glossary in the logic analysis system's online help.

Bus A bus is a group of associated signals within the logic analysis system.

Card A logic analyzer, oscilloscope, or pattern generator that can be inserted into a slot in logic analysis system frame. Cards can be combined with others to increase the channel count available in a single time domain.

Deskew To cancel or nullify the effects of differences between two different internal delay paths for a signal. Deskewing is normally done by running eye finder.

DUT Device Under Test—the board containing the baseband IC or peripheral device which you are testing.

Eye Finder A logic analyzer feature which trains the logic analyzer to sample each signal at the moment that it is most likely to be stable.

Intermodule Bus The intermodule bus (IMB) is a bus in the frame that allows the measurement modules to communicate with each other. Using the IMB, you can set up one instrument to *arm* another. Data acquired by instruments using the IMB is time-correlated.

Label See *Bus*.

Markers Markers are the green and yellow lines in the display that are labeled *x*, *o*, *G1*, and *G2*. Use them to measure time intervals or sample intervals. Markers are assigned to patterns in order to find patterns or track sequences of states in the data. The x and o markers are local to the immediate display, while G1 and G2 are global between time correlated displays.

Master Card In a module, the master card controls the data acquisition or output. The logic analysis system references the module by the slot in which the master card is plugged. For example, a 5-card Agilent Technologies 16555D would be referred to as Slot C: machine because the master card is in slot C of the mainframe. The other cards of the module are called expansion cards.

Module A logical collection of logic analyzer cards that are connected together. This gives you the flexibility to increase channel count by using more than one card. A module can be a single card or several cards, and a single card or several card module can be split into two modules. By definition, a module consists of a single time domain. While a module can consist of a single card, a module is not a physical entity. When a module has more than one card, one card is set up as the *master card*.

Pod Each of the cables coming out of the logic analyzer card is called a **pod**.

Probe A device to connect the various instruments of the logic analysis system to the device under test.

The word “probe” is used in three ways in this manual:

- The Agilent N4851A/B digital acquisition probe and N4861A/B digitial stimulus probe are always referred to as “acquisition probe” and “stimulus probe,” respectively.

- An Agilent probe connects the cables from the logic analyzer to the Samtec connectors on the N4851A/B acquisition probe. This probe is referred to as a “probe adapter.”
- An Agilent probe connects the N4851A/B acquisition probe to your DUT. This is referred to as a “probe.”

Probe Adapter See *probe*.

Sample Position The position of the logic analyzer’s setup/hold window for a particular channel, relative to the bus clock.

Skew Skew is the difference in channel delays between measurement channels. Typically, skew between modules is caused by differences in designs of measurement channels, and differences in characteristics of the electronic components within those channels. You should adjust measurement modules to eliminate as much skew as possible so that it does not affect the accuracy of your measurements.

State Measurement In a state measurement, the logic analyzer is clocked by a signal from the system under test. Each time the clock signal becomes valid, the analyzer samples data from the system under test. Since the analyzer is clocked by the system, state measurements are synchronous with the test system.

Storage Qualification Storage qualification is only available in a state measurement, not timing measurements. Store qualification allows you to specify the type of information (all samples, no samples, or selected states) to be stored in memory. Use store qualification to prevent memory from being filled with unwanted activity such as no-ops or wait-loops. To set up storage qualification, use “Trigger and fill memory with Default Storage” in a logic analyzer trigger sequence. In contrast, filters can hide data after it has been collected.

Symbol Symbols represent patterns and ranges of values found on logic analyzer buses. Symbols come from several sources:

1. Object file symbols — Symbols from your source code, and symbols generated by your compiler. Object file symbols may represent global variables, functions, labels, and source line numbers.
2. User-defined symbols — Symbols you create.
3. Predefined symbols — Symbols defined in a supplied configuration file.

Target System The device under test.

Timing Measurement In a timing measurement, the logic analyzer samples data at regular intervals according to a clock signal internal to the timing analyzer. Since the analyzer is clocked by a signal that is not related to the system under test, timing measurements capture traces of electrical activity over time. These measurements are *asynchronous* with the test system.

Trace All of the data captured by a run of the logic analyzer. Also called an “acquisition.”

Trigger Trigger is an event that occurs immediately after the instrument recognizes a match between the incoming data and the trigger specification. Once trigger occurs, the instrument completes its *acquisition*, including any store qualification that may be specified.

Trigger Sequence A trigger sequence is a sequence of events that you specify. The logic analyzer compares this sequence with the samples it is collecting to determine when to *trigger*.

Trigger Specification A set of conditions that must be true before the instrument triggers. See the printed or online documentation of your logic analyzer for details.

Y Adapter Cable See *probe*.

10 Glossary

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